GENERATING MULTIPLE BANDGAPS USING MULTIPLE EPITAXIAL LAYERS

BACKGROUND OF THE INVENTION

[0001] The present invention relates to quantum well intermixing (QWI) techniques suitable for modifying an energy bandgap during the formation of optical semiconductor devices. In particular, the invention relates to QWI techniques in which spatial control of the QWI process can be effected so as to achieve differing bandgap shifts across a wafer, device or substrate surface.

[0002] A vast body of research exists in the field of QWI. The QWI process consists in the selective disordering of the composition of the thin layers that form quantum wells, which results in a change of energy levels within each well causing the energy bandgap to shift. This allows one to alter the emission and absorption wavelengths of the intermixed material.

[0003] A variety of QWI techniques have been developed including : impunity- induced, impurity-free (dielectric cap), implantation-induced and laserinduced methods. QWI has been demonstrated in a range of material systems, including GaAs/AlGaAs and InP/(Al) InGaAs (P).

[0004] Much effort recorded in the prior art (prior art references are given in the Annex to this description, as referred to in square parentheses) has been directed to achieving a dual-bandgap process, where the emphasis is on obtaining a large differential shift between areas of reduced shift (nominally the as-grown bandgap) and intermixed areas. Various techniques have been proposed to enhance control over bandgap shifts, e. g.

varying the material [1, 2], deposition conditions [3,4], stoichiometry [5], size [6] and thickness [7-9] of the dielectric cap in impurity-free processes; ion irradiation dose [8, 10], laser exposure [11-14], surface coverage/resolution effects [15], and, most commonly, anneal temperature and duration in almost all of the above reports. Not all of these approaches, however, can be used to create multiple bandgap shifts on a single wafer-by temperature adjustment alone one cannot obtain more than one shift.

[0005] Most generally, multiple bandgaps can be created using a core dual-bandgap process with one of the following approaches:

[0006] 1. Repeated [10, 15-21] / variable dose [12-14] exposure-anneal combinations;

[0007] 2. Choice of dielectric caps of different material [2-5] and interface effects [1, 22-24];

[0008] 3. QWI barrier masks [7,9, 25, 26] and caps of varying thickness [7,8] ; and

[0009] 4. Spatial/resolution effects [6,15].

[0010] Despite the abundance of QWI techniques, there is a scarcity of prior art where these techniques could be used in a controlled manner to define multiple bandgap shifts on a common substrate.

[0011] A first prior art approach comprises various techniques where the rate of intermixing is controlled via the thickness of a barrier between the material being intermixed and the intermixing agent. The barrier may take the form of a mask or a

backspace layer. The intermixing agent may be in the form of a dielectric cap containing an impurity source, or an ion beam directed at the material being intermixed.

[0012] These techniques are typified in the general approach marked as 3 above (Paragraph [0008]), which places a common requirement for highly accurate controllability of the barrier thickness and its composition in order to achieve target bandgaps.

[0013] A second prior art approach exemplified in [26] proposes that a stack of alternating layers of two different materials that can be selectively etched is first deposited on the sample. Selective etching is then performed to remove a given number of layers from the stack in various regions of the sample. Ion implantation, followed by a high-temperature anneal, is then used to induce intermixing, with regions capped by a different number of layers experiencing different bandgap shifts. Reference [26] proposes deposition of metal layers by evaporation or sputter deposition to form the stack of alternating layers. In particular, a copper and titanium alternating layer system is recommended. A chromium and silicon system described is reported to result in significant problems in silicide formation at the interface between the two materials, which silicide inhibited etching of the chromium layers.

[0014] Selective etching of alternate InP/InGaAs semiconductor layers has been reported in [28], for the purpose of precision depth control in the fabrication of a variable-width core waveguide laser. This technique, often referred to as stepped, or staircase etching, is employed for the definition of spot-size converters, mode expanders and tapered

waveguides [29]. No suggestion of use of these layers as a QWI barrier has been proposed.

[0015] The group of references [1, 2, 22-24] marked as 2 above (Paragraph [0007]), and ~~patent~~ reference [30], are related to the use of composition of a topmost semiconductor layer and that of the dielectric cap, to control the bandgap shift in underlying areas. However, there is no suggestion of stacking or etching these barrier layers.

[0016] It is an object of the present invention to provide an improved QWI process that is capable of providing multiple bandgap shifts on a single device substrate, using a stack of alternating semiconductor layers that can be selectively etched and which provide a varying thickness barrier between a material to be intermixed and an intermixing agent.

[0017] According to one aspect, the present invention provides a method for producing multiple quantum well intermixed (QWI) regions having different bandgaps on a single substrate, comprising the steps of: forming a substrate comprising one or more core layers defining at least one quantum well; depositing a succession of intermixing barrier layers over the quantum well, each successive intermixing barrier layer being formed of a semiconductor material and having a different etch characteristic than an immediately preceding barrier layer; etching away different numbers of the successive barrier layers in different regions of the substrate so as to provide different total thicknesses of barrier layer in different regions of the substrate; and applying an intermixing agent to the surface of the substrate such that the degree of intermixing in the quantum well region varies as a function of the total thickness of barrier layer, thereby forming different bandgaps in the quantum well in each of the respective regions.

[0018] According to another aspect, the present invention provides a semiconductor optical device manufactured using the process defined above.

[0019] According to another aspect, the present invention provides a wafer of epitaxially grown material comprising a mechanically supporting substrate, one or more layers defining a quantum well structure deposited thereon, and a succession of intermixing barrier layers formed over the quantum well structure, each successive intermixing barrier layer being formed of a semiconductor material having a different etch characteristic than an immediately preceding barrier layer so that each successive layer can act as an etch stop layer to an immediately preceding higher layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Embodiments of the present invention will now be described by way of example and with reference to the accompanying drawings in which:

[0021] Figures 1A-1L are ~~is a~~ schematic ~~diagram~~ cross sectional views of a device substrate during ~~various~~ successive stages of the QWI processing steps according to one embodiment of the present invention;

[0022] Figures 2A-2K are ~~is a~~ schematic ~~diagram~~ cross sectional views of a device substrate during ~~various~~ successive stages of the QWI processing steps according to another embodiment of the present invention; and

[0023] Figure 3 is a graph showing bandgap shifts, represented by photoluminescence wavelength shift, effected in different regions of the substrate arising from the processing steps as applied to the structures of ~~figure~~ Figures 1A-1L.

DETAILED DESCRIPTION

[0024] The process of the present invention allows multiple bandgaps to be defined in a controlled manner on the same wafer or substrate. The process is compatible, inter alia, with Al-quaternary InP material on a semi-insulating (SI) InP substrate, and thus can be used to fabricate high-frequency optoelectronic devices. This enables a plethora of component integration possibilities whereby active and passive components, each bandgap-tuned as required, can be fabricated on a common substrate as part of a photonic integrated circuit and/or a single integrated device. Examples include semiconductor optical amplifier (SOA)-preamplified modulators, photodetectors and switches, extended-cavity lasers, wavelength-detuned laser arrays, demultiplexers, etc.

[0025] For the avoidance of doubt, it is noted that throughout the present specification and particularly including the claims, for brevity and clarity the expression 'substrate' is used in a general sense to include the mechanically supporting and 'original' substrate and all further material layers in existence above that original substrate at the time of a subsequent process step. In other words, the expression 'substrate' is intended to cover the totality of previously processed material and layers to which a process or further process (e. g. layer deposition or thermal treatment) is to be applied.

[0026] The original 'raw material' substrate will be referred to as the mechanically supporting substrate, although it will be understood that this too may change its physical and chemical characteristics during processing.

[0027] The process of the present invention allows multiple bandgaps to be defined in a controlled manner on the same wafer or substrate, by way of barrier thickness control

through the sequential reduction of a stack of alternating ingrown epitaxial layers of different materials that are capable of being selectively etched over each other.

[0028] In a preferred embodiment, the process is implemented using custom-designed epitaxial wafer material having a sacrificial cap of alternating semiconductor layers. The number of layer pairs in the stack is two fewer than the total number of bandgaps required (i.e. including the as-grown one), whilst thicknesses and compositions of individual layers determine the shifts obtainable with stacked combinations of these layers. The composition of the topmost layer should, but does not have to, be the same as that of the bottom-most layer.

[0029] Figures 1A-1L show[[s]] a process flow for intermixing Al-quaternary InP material to create four different bandgaps. The as-grown wafer structure includes an InP mechanically supporting substrate 10 which includes any cladding layers and one or more quantum well layers required to define and form an active waveguide core (hereinafter 'core layers'). These layers are formed in the Al-quaternary materials in accordance with known techniques in the fabrication of optoelectronic devices, and will not be described further here.

[0030] Above the core layers are provided first and second cap layers 11,12 respectively in InGaAs and InGaAlAs, the preferred functions of which layers will be explained later.

[0031] Above these layers is provided a layered structure of intermixing barrier layers 20 to 24, comprising two repeats of an InGaAs/InP layer pair 21,22 and 23,24 with an underlying InGaAs layer 20. The wafer structure below the underlying barrier layer 20

depends on a choice of surface planarization techniques and ohmic contact requirements. These will be discussed later.

[0032] The alternating InGaAs and InP layers 20 to 24 are selected to provide differential etch properties, so that each layer can be etched using the lower layer as an effective etch stop. Selective wet etching using two different etch solutions is employed to etch one layer and stop on the other in an alternating fashion. For the specific embodiment described here, recommended etch recipes are:

[0033] Recipe 1 : H_3PO_4 : H_2O_2 : H_2O (1 : 1: 38); selectively etches InGaAs over InP

[0034] Recipe 2: HCl : H_2O (3: 1); selectively etches InP over InGaAs.

[0035] In another example, the etch recipes may be:

[0036] Recipe 1: H_2SO_4 : H_2O_2 : H_2O (1: 8 : 40); selectively etches InGaAs over InP

[0037] Recipe 2: HCI : H_3PO_4 (1: 3); selectively etches InP over InGaAs.

[0038] In a first step, the substrate in ~~figure~~ Figure 1A[[1-1]] is photolithographically patterned to expose the surface in first and second regions corresponding to what will become the two largest bandgaps BG3 and BG2 (see ~~figures~~ Figures 1G[[1-7]] to 1L[[1-12]]). The topmost InGaAs layer 24 is then selectively etched using Recipe 1. The etch mask is removed leaving the substrate as shown in ~~figure~~ Figure 1B[[1-2]].

[0039] The underlying InP layer 23 is selectively etched using Recipe 2 to leave the substrate as shown in ~~figure~~ Figure 1C[[1-3]].

[0040] The substrate is then photolithographically patterned to expose the surface in the first regions corresponding to what will become the largest bandgap region (BG3-as seen in ~~figure~~ Figure 1G[[7]] to 1L[[12]]). The InGaAs layer 22 is selectively etched using Recipe 1. The etch mask is removed leaving the substrate as shown in ~~figure~~ Figure 1D[[1-4]].

[0041] The underlying InP layer 21 is selectively etched using Recipe 2 to leave the substrate as shown in ~~figure~~ Figure 1E[[1-5]].

[0042] The substrate is then covered with a blanket layer of a QWI-suppressing material 30, such as PECVD silica. The substrate is then photolithographically patterned to protect the regions of suppressed or zero bandgap shift, shown as BG0 in ~~figure~~ Figure 1G[[1-7]] to 1L[[1-12]] (i.e. the regions of 'as-grown' bandgap). The silica 30 is then either dry-etched or wet-etched in the exposed areas (BG1, BG2, BG3) with an HF-based solution. The etch mask is removed leaving the substrate as shown in ~~figure~~ Figure 1F[[1-6]].

[0043] An intermixing agent, in the form of an intermixing cap or QWI-initiating layer 40, is deposited over the entire substrate surface to leave the substrate as shown in ~~figure~~ Figure 1G[[1-7]]. The QWI-initiating layer 40 preferably consists of a sputter deposited layer of impurity and of silica. The impurity may be any one or more of sulphur, zinc, silicon, fluorine, copper, germanium, tin and selenium. The impurity may be incorporated within the silica layer as a doping impurity, or may formed as a separate impurity layer above, below or within the silica layer.

[0044] The substrate is then intermixed by way of a thermal process, preferably a high-temperature rapid thermal anneal. As shown in ~~figure~~ Figure 1G[[1-7]], the bandgaps

BG1 to BG3 are created during this step. Bandgap BG0 corresponds to the as-grown (native) bandgap, which is preserved during the thermal process.

[0045] A typical rapid thermal anneal process may be performed between 600 and 700 degrees C. The temperature and duration of the rapid thermal anneal step may be selected in order to achieve the required bandgap shifts.

[0046] The QWI-initiating layer 40 is then removed, together with any silica layer 30, for example by wet etching using an HF-based etchant. The exposed upper layer 24 of InGaAs together with any exposed regions of impurity-rich barrier layer 20 are removed by dry etching and the topmost portion of the second cap layer 12 may also be removed by over-etching of the barrier layer 20. This leaves the substrate as shown in ~~figure~~ Figure 1H[[1-8]].

[0047] At this stage, the process for forming multiple quantum well intermixed regions having different bandgaps is complete. However, under many circumstances, it is desirable to planarize the surface of the substrate prior to further processing for device fabrication. For example, the formation of optical waveguides may require etching of the surface of the cap layers 11, 12 and it is desirable to perform these fabrication steps starting from a relatively planar substrate.

[0048] One presently preferred process for planarization is shown with reference to ~~figures~~ Figures 1I[[1-9]]to 1L[[1-12]]. For best effect, the second cap layer 12 is chosen to have high etch resistance to both recipes 1 and 2, thereby acting as a common etch-stop layer. This way, the alternating wet etching routine can be continued after the bandgap shifting process until the remainder of the intermixing barrier layers 20 to 24

have been completely removed. The etching process will stop on the second cap layer 12. For this reason, the second cap layer, or common etch-stop layer 12 is preferably formed from InGaAlAs. InGaAlAs is known to have variable etchability in Recipes 1 and 2 depending on the mole fractions of the constituent elements and volume parts of the wet etch ingredients. By adjusting these parameters, the required selectivity can readily be achieved so that the InGaAlAs layer 12 is not attacked during etching of the lower InGaAs layer 20.

[0049] Other options include using different etch chemistries to etch the InP and InGaAs layers 20 to 24, which etches are selected not to etch the InGaAlAs common etch-stop layer 12. For example, citric acid-based solutions ($C_6H_8O_7$: H_2O_2) exhibit different etch selectivities for a range of volume part ratios ~~[31]~~.

[0050] In another alterative, instead of an InGaAlAs layer, one can employ an ultra-thin AlAs common etch stop layer 12 (several monolayers thick), which has been shown to be a reliable etch-stop layer in InP/InGaAs material systems ~~[32]~~.

[0051] Using a common etch-stop layer 12, the uppermost InP layer 23 is removed using etch Recipe 2, leaving the substrate as shown in ~~figure~~ Figure 1I[[1-9]]. The uppermost InGaAs layer 22 is then removed using etch Recipe 1 to leave the substrate as shown in ~~figure~~ Figure 1J[[1-10]]. The uppermost InP layer 21 is then removed using etch Recipe 2 to leave the substrate as shown in ~~figure~~ Figure 1K[[1-11]].

[0052] The remaining parts of the InGaAs layer 20 are then removed using etch Recipe 1, leaving the common etch-stop layer 12, as shown in ~~figure~~ Figure 12. Finally, this common etch-stop layer 12 can then removed by either dry etching or appropriate wet-

etching, leaving a standard InGaAs contact layer 11 as the uppermost layer of the substrate. The device fabrication cycle can then continue in a conventional known manner suitable for manufacture of desired optoelectronic devices.

[0053] In some circumstances, it may be desirable to avoid using a planarization etch-stop layer 12, for example, where this interferes with the migration of intermixing impurities into the main body of the substrate from the QWI- initiating layer 40. In these circumstances, an alternative planarization process may be used which makes use of a replica stack of InP / InGaAs layers 50 to 54, below the main InP / InGaAs layers 20 to 24, as shown in ~~figure~~ Figure 2. This replica stack of layers 50 to 54 is identical in layer sequence and preferably identical in chemistry to the main stack of InP / InGaAs layers 20 to 24. However, in the replica stack, the layer thicknesses are much thinner, preferably to an extent that the existence of residual portions of the stack in various regions of the substrate will not cause difficulties in subsequent processes.

[0054] With reference to ~~figure~~ Figures 2A-2K, the alternative planarization process is now described. The replica stack of layers 50 to 54 is shown in ~~figure~~ Figure 2A[[2-1]]. Note that the uppermost InGaAs layer 54 of the replica stack is effectively the same layer as, or contiguous with, the lowermost InGaAs layer 20 of the main barrier layer stack. Similarly, the lowermost InGaAs layer 50 of the replica stack is effectively the same layer as, or contiguous with, the InGaAs cap layer 11 of the main body of the substrate.

[0055] The main barrier layers 20 to 25 are typically of the order of several hundred nanometres thick, or even up to 1 micron thick. The layer thickness of these barrier layers is determined by the requirements of the QWI process used, in that the individual layer

thicknesses must be sufficient to suppress migration of impurities to the quantum well to the extent necessary to achieve the correct bandgap shifts. However, the replica stack layers 50 to 54 should consist only of thin etch-stop layers of the order of, typically, 20 to 30 nm thickness. As will become clear, the thickness of each of these layers should be sufficient to resist substantial over-etching periods of the adjacent upper layer, but insufficiently thick to (a) cause planarity problems after the QWI process is completed, and (b) significantly reduce the local effectiveness of the QWI process.

[0056] The first processing stages are carried out in corresponding manner to those described with reference to ~~figures~~ Figures 1A [[1-1]] to 1F[1-6]]. Therefore, upon completion of the barrier layer processing steps shown with reference to ~~figures~~ Figures 1A [[1-1]] to 1F[1-6]], applied to the substrate of ~~figure~~ Figure 2A[[2-1]], a corresponding result is shown in ~~figure~~ Figure 2F[[2-6]]. See Figures 2B-2E. ~~(Corresponding figures 2-2 to 2-5 are omitted for conciseness.)~~

[0057] An intermixing agent, in the form of an intermixing cap or QWI-initiating layer 40, is deposited over the entire substrate surface to leave the substrate as shown in ~~figure~~ Figure 2G[[2-7]]. The QWI-initiating layer 40 preferably consists of a sputter-deposited layer of impurity and of silica as previously described.

[0058] The substrate is then intermixed by way of a thermal process, preferably a high-temperature rapid thermal anneal. As shown in ~~figure~~ Figure 2G[[2-7]], the bandgaps BG1 to BG3 are created during this step. Bandgap BG0 corresponds to the as-grown (native) bandgap.

[0059] The QWI-initiating layer 40 is then removed, together with any silica layer 30, for example by wet-etching using an HF-based etchant. The exposed upper barrier layer 24 of InGaAs together with any exposed regions of barrier layer 20 (replica layer 54) are removed by dry or wet etching. This leaves the substrate as shown in ~~figure~~ Figure 2H[[2-8]].

[0060] To planarize the surface, the barrier layer 23 is removed with an appropriate wet etch recipe which will also remove the thin replica layer 53. However, although the thin replica layer will be subject to a substantial overetch period sufficient to remove the thicker barrier layer 23, the etch-stop layer 52 will prevent further etching of the substrate in the BG3 region. The result is shown in ~~figure~~ Figure 2I [[2-9]]. An appropriate etch recipe is then used to remove barrier layer 22 and, correspondingly, replica layer 52, the etch stopping on layers 21 and 51 to leave the substrate as shown in ~~figure~~ Figure 2J[[2-10]]. Subsequently, an appropriate etch process removes layers 21 and 51 to leave the substrate as shown in ~~figure~~ Figure 2K[[2-11]].

[0061] Although some or all of the replica layers 50 to 54 are still present in certain regions of the substrate, because these replica layers are very thin (e. g. between one and two orders of magnitude thinner than the removed barrier layers 20 to 24), there is little difficulty with subsequent device processing steps. The resulting replica stack is preferably less than 100 nm thick in its highest regions. Such height non-uniformity across the sample surface is acceptable, especially if a further etch-stop process is used later in the processing, e. g. to define the etch depth of optical waveguides.

[0062] Other approaches may include the use of an extra-thick InP buffer layer ~~12'~~ (instead of cap layer 12, ~~figure~~ Figure 1A[[1-1]]) as a buffer underneath the barrier layers 20 to 24. If the buffer layer ~~12'~~ is sufficiently thick so that some of it remains after the series of barrier definition etches, then the substrate can be planarized in a single extended wet etch step by reliance on the InGaAs cap layer 11 underneath the InP buffer.

[0063] It will be noted from ~~figures~~ Figures 1A-1L and Figures 2A-2K that each separate bandgap shift region of the substrate (BG1... BG3) is defined by a different number of barrier layer pairs (in the example, each pair comprising an InP layer and an InGaAs layer). In other words, region BG3 is protected by zero barrier layer pairs; region BG2 is protected by one barrier layer pair 21, 22; region BG1 is protected by two barrier layer pairs 21, 22,23, 24; while region BG0 is protected by an additional QWI-suppression cap. However, it will be understood that the technique could be practised by each separate region BG0... BG3 being protected with a respective number of single barrier layers, rather than barrier layer pairs. In this instance, each successive barrier layer must provide (i) the requisite increased resistance to bandgap shift in underlying areas during the QWI process; and (ii) the necessary etch stop chemistry for removal of the immediately higher barrier layer.

[0064] The bar chart of Figure 3 shows the bandgap shifts observed experimentally in Al-quaternary MQW InP material intermixed using such a process. The barrier layer structure is represented with the following codes: "A" represents an InP layer, and "B" represents an InGaAs layer.

[0065] As is evident from Figure 3, differential bandgap shifts can be obtained in three ways: (i) exploitation of the interface effect of the material of the topmost layer in contact with the QWI-initiating cap 40 (e. g. , A vs. AB, AB vs. ABA, ABA vs. ABAB); (ii) the effect of the stack thickness for an identical topmost layer (A vs. ABA and AB vs. ABAB); and (iii) the number of interfaces and the sequence of layers within the barrier layer stack. Thus, it will be understood that the 'resistance to bandgap shift' afforded by a barrier layer 20 to 24 may be a function not only of the thickness of the barrier layer, but also of its interaction with the QWI-initiating cap (i. e. the surface interface effects at the boundary between the two materials, and also of the number of layer interfaces within the barrier layer stack (i. e. the interface effects at boundaries within the barrier layer stack). It is noted that the techniques of the invention described herein are compatible with exploitation of both interface effects and barrier thickness effects to control a degree of QWI that takes place. Interface effects are described in references [1, 2, 22-24] and ~~patent~~ [30].

[0066] The paired barrier layer approach (marked by arrows in Figure 3, and as described in connection with ~~figures~~ Figures 1A-1L and 2A-2K), offers substantial advantages in view of maintaining identical QWI-initiating layer/barrier layer interface effects. These interface effects can be very significant in some QWI processes.

[0067] The paired barrier layer technique avoids any difficulties which may otherwise be caused by the requirement to use an etch chemistry that allows selective etch of the QWI-initiating layer against both the first and second barrier layer material types. In other words, in using a paired barrier layer technique, the removal of the QWI-initiating layer 40 (progressing from the substrate of ~~figure~~ Figure 1G[[1-7]] to the substrate of ~~figure~~

Figure 1H [[1-8]]) requires an etch that stops against the same material type (layers 20, 22 and 24).

[0068] Conversely, if only a single extra barrier layer is used for each successive region BG3 to BG1, then the removal of the QWI-initiating layer 40 has to stop against two or more different types of material. Thus, the selectivity of the etch chemistry of the topmost barrier layer relative to that of the QWI- initiating cap may also be considered when selecting either the single barrier layers approach or the paired barrier layers approach.

[0069] It will be understood that the processes described above can be extended in principle to any number of different bandgaps.

[0070] Although the exemplary embodiments above have been described in connection with an impurity-based QWI-initiating layer, other types of QWI-initiating materials and techniques may be used to initiate, accelerate or promote the intermixing process. These include impurity-free dielectric caps, sputtered materials (e. g. silica), plasma/sputter damage and some of the techniques outlined in the review of the prior art above. It is noted that the QWI-initiating layer processes described in connection with ~~figures~~ Figures 1A-1L and 2A-2K would be incompatible with the barrier layers proposed in reference [26]. QWI intermixing can also be induced by ion implantation.

[0071] In a general sense, it is noted that the QWI-initiating layer, or ion implantation, effectively provide a means for applying an intermixing agent (e. g. impurity) to the surface of the substrate. The expression [[']]"surface of the substrate[[']]" is intended to encompass ion implantation where substantial quantities of the introduced agent are actually driven past the surface.

[0072] In preferred embodiments, the application of the intermixing agent includes an intermixing agent activation step, such as the high temperature rapid thermal anneal process described above. Some QWI processes, for example photo-absorption-induced disordering, may require no activation step at all.

[0073] Although the exemplary embodiments above have been described in connection with a QWI-inhibiting layer of PECVD silica layer, other types of QWI-inhibiting materials may be used to inhibit, suppress or otherwise retard the intermixing process. These include spin-on glass, sputtered silica etc.

[0074] In practice, the QWI-inhibiting layer 30 might not be required at all in certain circumstances. In a first example, if the cumulative thickness of barrier layers 20 to 24 is sufficient to completely suppress QWI in the thickest region BG0, then the native as-grown bandgap BG0 will be retained in those areas. This technique could be particularly applicable where implantation is used for application of the QWI agent. In a second example, it might not be necessary to retain the native as-grown bandgap, i.e. the region BG0 might also be intentionally bandgap shifted. In a third example, where the presence of, for example, the InGaAs layer 24 at all interface with the QWI-initiating material is important to entrance migration of the QWI agent into the substrate, omission (i.e. removal) of this layer in the BG0 region may be sufficient to substantially depress migration of the QWI agent such that the remaining thickness of barrier layers 20 to 23 are themselves sufficient to effectively prevent QWI in region BG0. In this case, rather than depositing layer 30, the upper barrier layer might actually be removed in the BG0 regions. In a fourth example, the removal of QWI-initiating material in the BG0 region prior to the activation step (e. g., rapid thermal anneal) may prove sufficient to suppress

any bandgap shift in that region. The QWI-initiating cap in the BG0 region may be removed either by etching or lift-off using photolithography. In this case, the anneal conditions used to induce bandgap shifts in areas BG1-BG3 covered by the QWI-initiating cap must not affect the native bandgap in the-uncapped region BG0.

[0075] Embodiments of the invention offer a number of advantages. It is possible to create a large number of bandgap shifts of arbitrary magnitude and these can readily be altered. Multiple bandgap shifts can be achieved with only a single intermixing step, i.e. a single application/activation of a QWI initiating agent. Superior barrier layer thickness and composition control can be achieved by virtue of the use of epitaxially grown barrier layers, preferably using the same equipment as used for formation of the substrate quantum well structures.

[0076] Preferably, the barrier layers are formed in a continuous process sequence with the epitaxial growth of the underlying substrate quantum well structures (i. e. without removal of the wafer substrates from the vacuum deposition environment), guaranteeing high purity and low contamination. This is a substantial improvement over the provision of separately deposited, (evaporated or sputtered) metal barrier layers as proposed in reference [26].

[0077] Epitaxial growth of the barrier layers as described here ensures extremely good spatial uniformity of the layers, compositional control and near-atomic scale precision which ensure superior etch rate control and control of migration of the QWI initiating agent during the application/activation step.

[0078] Furthermore, the process is suitable for large-scale production because the barrier layer thicknesses and compositions can be incorporated into the as-grown wafers for later application of the QWI processes. No post-growth barrier layer deposition is necessary.

[0079] Further advantages can be realised in that the process described herein can be made fully compatible with a wide range of different materials systems including Al-quaternary InP material systems on a semi-insulating InP substrate. Planarization of the substrate after QWI processing can be effected without any further photolithography steps which reduces cost and potential yield losses.

[0080] Other embodiments are intentionally within the scope of the accompanying claims.

[0081] Annex 1 : References

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